Claims

What is claimed is:

1. A clock generator for generating a non-phase-modulated target clock signal based on a phase-modulated input signal, the clock generator comprising:
an operation circuit for calculating a cycle value by calculating the number of cycles of an oscillating signal during a cycle of the input signal and for comparing the cycle value with a critical value for outputting a first protection signal; and
a phase-locked loop connected to the operation circuit for generating the target clock signal according to the first protection signal and the input signal, feeding the target clock signal back to the input of the phase-locked loop, and determining whether the target clock signal is to be synchronized with the input signal based on the logic level of the first protection signal;
wherein the target clock signal is generated based on the oscillating signal, when the first protection signal corresponds to a first logic level, the phase-locked loop compares the target clock signal with the input signal to drive the target clock signal to be synchronized with the input signal, and when the first protection signal corresponds to a second logic level, the phase-locked loop holds the target clock signal without driving the target clock signal to be synchronized with the input signal.

2. The clock generator of claim 1, wherein the operation circuit comprises:
a counter for calculating the cycle value by calculating a number of cycles of the oscillating signal during a cycle of the input signal; and
a comparator connected to the counter for comparing the cycle value with a preset cycle value to generate a first protection signal.

3. The clock generator of claim 2, wherein the phase-locked loop comprises:
a phase-frequency detector connected to the comparator for outputting a control signal by comparing the target clock signal with the input signal and for

determining whether to compare the target clock signal with the input signal based on the logic level of the first protection signal;

a loop filter connected to the phase-frequency detector for generating a control voltage based on the control signal; and

a voltage-controlled oscillator connected to the loop filter for controlling the frequency of the target clock signal based on the control voltage.

4. The clock generator of claim 3, wherein the phase-locked loop further comprises:

a frequency divider connected to the voltage-controlled oscillator for lowering the frequency of the oscillating signal to generate the target clock signal; and

a second slicer connected to the frequency divider and the phase-frequency detector for slicing the target clock signal.

5. The clock generator of claim 3, wherein the clock generator further comprises:

a band-pass filter for extracting the input signal having a frequency within a predetermined band; and

a first slicer connected to the band-pass filter for slicing the input signal and forwarding the input signal to the counter of the operation circuit and the phase-frequency detector of the phase-locked loop.

6. The clock generator of claim 1, wherein when the difference between the cycle value and the preset cycle value is not larger than a critical value, the first protection signal is set to a first logic level.

7. The clock generator of claim 1, wherein when all the differences between a plurality of the consecutive cycle values and the preset cycle value are not larger than a critical value, the first protection signal is set to a first logic level.

8. The clock generator of claim 1, wherein when the difference between the cycle value and the preset cycle value is larger than a critical value, the first protection signal is set to a second logic level.

9. The clock generator of claim 1, wherein when all the differences between a plurality of the consecutive cycle values and the preset cycle value are larger than a critical value, the first protection signal is set to a second logic level.

10. The clock generator of claim 1 being applied to an optical drive, wherein the optical drive is a DVD-R optical drive or a DVD-RW optical drive, the optical drive comprising an ADIP decoder for predicting a timing for the input of the first period corresponding to the next ADIP unit of the input signal and generating a second protection signal to prohibit the phase-locked loop from driving the target clock signal to be synchronized with the input signal at a predetermined time before the timing of the input of the first period corresponding to the next ADIP unit of the input signal.

11. A clock generating method for generating a non-phase-modulated target clock signal based on a phased-modulated input signal,

the clock generating method comprising:

determining whether the target clock signal is to be synchronized with the input signal according to a first protection signal for generating a control signal;

generating a control voltage based on the control signal; and

controlling the frequency of the target clock signal according to the control voltage;

wherein a cycle value is generated by calculating the number of cycles of an oscillating signal during a cycle of the input signal and the logic level of the first protection signal is determined by comparing the cycle value with a preset cycle value.

12. The clock generating method of claim 11, wherein the generating method further comprises:

receiving the input signal and the oscillating signal to calculate the number of cycles of an oscillating signal during a cycle of the input signal; and

generating a first protection signal by comparing the cycle value with a preset cycle value.

13. The clock generating method of claim 11, wherein when the first protection

signal equals to a first logic level, the method further comprises comparing the target clock signal with the input signal for driving the target clock signal to be synchronized with the input signal, and when the first protection signal equals to a second logic level, the method further comprises holding the target clock signal without driving the target clock signal to be synchronized with the input signal.

14. The clock generating method of claim 13, wherein when the difference between the cycle value and the preset cycle value is not larger than a critical value, the first protection signal is set to a first logic level.

15. The clock generating method of claim 13, wherein when all the differences between a plurality of the consecutive cycle values and the preset cycle value are not larger than a critical value, the first protection signal is set to a first logic level.

16. The clock generating method of claim 13, wherein when the difference between the cycle value and the preset cycle value is larger than a critical value, the first protection signal is set to a second logic level.

17. The clock generating method of claim 13, wherein when all the differences between a plurality of the consecutive cycle values and the preset cycle value are larger than a critical value, the first protection signal is set to a second logic level.

18. The clock generating method of claim 11 being applied to an optical drive, wherein the optical drive is a DVD-R optical drive or a DVD-RW optical drive, the clock generating method further comprising predicting a timing for the input of the first period of the input signal and generating a second protection signal to hold the target clock signal without driving the target clock signal to be synchronized with the input signal at a predetermined time before the timing of the input of the first period of the input signal.

19. The clock generating method of claim 18 further comprising disabling the second protection signal when the prediction of the timing for the input of the first period of

the input signal functions incorrectly.